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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,827	WEIS ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-12 and 45-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-12 and 45-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicants' amendment filed on March 29, 2006. Claims 1-6,13-44 were cancelled. Claims 7-12,45-51 are pending, in which claims 45-51 have been newly added.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

1. Claims 7-12,45-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman et al (6,339,241).

Re claim 7, Mandelman teaches a memory cell structure for a memory cell array comprised of a plurality of the memory cells arranged in rows and columns, the memory cell comprising: at least two deep trench structures 24,26 (Fig 5, col 5, lines 20-52; Figs 1-4, 10d) formed in a semiconductor substrate, and along one of the rows, each of the deep trench structures comprising a deep trench defined in the semiconductor substrate, the deep trench having first and second sidewalls extending along a bottom region, a middle region, and an upper region, a dielectric film 32 extending along the first and second sidewalls of the bottom region of the deep trench, a first trench-collar portion 30 extending along the first sidewalls of the middle region and a second trench-collar portion 28 extending along the second sidewalls of both the middle and upper regions; at least two isolation trenches adjoining the two deep trench structures, each of the isolation trenches extending across the memory cell array such that at least one active area 44 is defined by the at least two isolation trenches and by the at least two deep trenches 24,26 (Fig 5); and polysilicon 34 filling the bottom and middle regions of the deep trenches 24,26 (Fig 5; col 5, lines 20-52). Re claim 8, wherein the at least two deep trench structures are separated by a distance 3F, where F is a minimum feature size (Figs 1-4; col 2, lines 35-60; col 4, lines 1-44; col 5, liens 1-10). Re claim 9, wherein the at least an upper portion of the polysilicon 34 filling the middle region is doped polysilicon and further comprising a trench top oxide 36 formed atop the doped polysilicon; a gate dielectric layer 42 formed along the first sidewalls of the upper region of the deep trench; and a buried strap region 38 in the semiconductor substrate adjoining the first sidewalls, adjacent the doped polysilicon and below the trench top oxide 36 (Fig 5; col 5, lines 20-52; Figs 6-7; col 6, line 10 through col

7). Re claim 10, wherein the buried strap region 38 of each of the plurality of the memory cells adjoining a same side of the deep trenches 24,26 (Figs 1-5,10d; col 5, lines 12-52). Re claim 11, wherein the buried strap region 38 of the adjacent ones of the plurality of the memory cells adjoining opposite side of its deep trenches (Figs 1-5,10d; col 5, lines 12-52). Re claim 12, further comprising: a further polysilicon layer 40 atop the trench top oxide layer 36; a doped region 46,48 formed in a top surface of the semiconductor substrate adjacent to the gate dielectric layer 42; a contact region 52to the further polysilicon layer that connects the further polysilicon layer to a word line 1; and another contact region to the doped region that connects the dope region to a bit line 3 (Figs 5,1-4,10d; col 5, lines 1-52; Figs 6-7; col 6, line 1 through col 7). Re claim 45, wherein the bottom region of the deep trenches are formed in heavily doped or buried plate region 22 of the semiconductor substrate such that the buried plate region, the dielectric layer 32 covering the sidewalls of the bottom region of the deep trench and the polysilicon 34 filling the bottom region of the deep trenches comprise the capacitor first plate, the capacitor dielectric and the capacitor second plate of a memory cell capacitor respectively (Fig 5, col 5, lines 20-52; col 2, line 49 through col 4). Re claim 46, the structure further comprising: a trench top oxide 36 formed atop the polysilicon 34 that fills the middle region of the deep trench, a further polysilicon layer 40 atop the trench top oxide layer; a doped region 46,48 formed in a top surface of the semiconductor substrate adjacent to the deep trench; a contact region 52 to the further polysilicon layer that connects the further polysilicon layer to a word line 1; another contact region to the doped region that connects the doped region to a bit line 68,3; and a transistor having first and second source/drain connections 46,48,38 and a gate connection 40, the gate connection connected to the further polysilicon and the word line 1, one of the first and second source/drain connections connected to the doped region and the bit line of the other one of the first and second source/drain 38 electrically connected to the polysilicon 34 that fills the bottom region of the deep trench that comprises the second plate of a memory cell capacitor (Figs 5,1-4,10d; col 5, lines 1-52; Figs 6-7; col 6, line 1 through col 7). Re claim 47, the structure further comprising: a transistor having first and second source/drain connections 46/48,38 and a gate connection 40, the gate connection connected to the further polysilicon 40 and the word line 1, one of the first and second source/drain connections connected to the doped region and the bit line 68,3 of the other one of the first and second

source/drain electrically connected to the polysilicon that fills the bottom region of the deep trench that comprises the second plate of a memory cell capacitor (Figs 5,1-4,10d; col 5, lines 1-52; Figs 6-7; col 6, line 1 through col 7; col 2, line 12 through col 4). Re claim 48, wherein the doped region 46/48 is the first source/drain, the buried strap 38 is the second source/drain, and further polysilicon 40 is the gate of a vertical transistor (Fig 5; col 5, lines 20-52). Re claims 49-51, wherein at least two deep trench structures are separated by a distance 3F, where F is a minimum feature size (Figs 1-4; col 2, lines 35-60; col 4, lines 1-44; col 5, liens 1-10).

Claim Rejections - 35 USC § 103

2. Claims 7-12,45-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arnold et al (2004/0238868) taken with Mandelman et al (6,339,241).

Arnold teaches (at Figures 1-7,14C-21; paragraphs 40-90) a memory cell structure for a memory cell array comprised of a plurality of the memory cells arranged in rows and columns (Figs 1A,2,3,7,14C-21C) the memory cell comprising: at least two deep trench structures 20 (Fig 2; paragraphs 45-51) formed in a semiconductor substrate, and along one of the rows, each of the deep trench structures comprising a deep trench defined in the semiconductor substrate, the deep trench having first and second sidewalls extending along a bottom region, a middle region, and an upper region, a dielectric film extending along the first and second sidewalls of the bottom region of the deep trench, a first trench-collar portion extending along the first sidewalls of the middle region and a second trench-collar portion extending along the second sidewalls of the middle region (Figs 2,3,4A,4B); and at least two isolation trenches 10 adjoining the two deep trench structures (Figs 2,3), each of the isolation trenches extending across the memory cell array such that at least one active area 6 is defined by the at least two isolation trenches 10 (Fig 3) and by the at least two deep trenches; and polysilicon 20,50 filling the bottom and middle regions of the deep trenches (Figs 1A,2,3,7,14C-21C; paragraphs 45-51;84-90). Re claim 8, wherein the at least two deep trench structures 20 are separated by a distance 3F, where F is a minimum feature size (see Fig 2). Re claim 9, wherein the at least an upper portion of the polysilicon filling the middle region is doped polysilicon (Fig 2, paragraphs 46-47) and further comprising a trench top oxide 32 formed atop the doped polysilicon; a gate dielectric layer 36 formed along the first sidewalls of the upper region of the deep trench; and a

buried strap region 28 in the semiconductor substrate adjoining the first sidewalls, adjacent the doped polysilicon and below the trench top oxide 32 (Figs 2,3; paragraphs 46-47). Re claim 10, wherein the buried strap region 28 of each of the plurality of the memory cells adjoining a same side of the deep trenches 20 (Figs 2-3). Re claim 11, wherein the buried strap region 28 of the adjacent ones of the plurality of the memory cells adjoining opposite side of its deep trenches 20 (Figs 2-3). Re claim 12, further comprising a further polysilicon 34 layer atop the trench top oxide layer 32 (Figs 2,3,4C); a doped region 38 (2,3,6C) formed in a top surface of the semiconductor substrate adjacent to the gate dielectric layer; a contact region to the further polysilicon layer that connects the further polysilicon layer to a word line; and another contact region to the doped region that connects the dope region to a bit line (Figs 2-3; 6C-6I). Re claim 45, wherein the bottom region of the deep trenches are formed in heavily doped or buried plate region 26 of the semiconductor substrate such that the buried plate region 26, the dielectric layer 29 covering the sidewalls of the bottom region of the deep trench and the polysilicon filling the bottom region of the deep trenches comprise the capacitor first plate, the capacitor dielectric and the capacitor second plate of a memory cell capacitor respectively (Fig 2, paragraph 46). Re claim 46, the structure further comprising: a trench tap oxide 32 formed atop the polysilicon 34 that fills the middle region of the deep trench (Figs 2-3,4C; paragraphs 46-46) a further polysilicon layer atop the trench top oxide layer 32; a doped region 38 (Figs 2,3,6C) formed in a top surface of the semiconductor substrate adjacent to the deep trench; a contact region to the further polysilicon layer that connects the further polysilicon layer to a word line; another contact region to the doped region that connects the dope region to a bit line (Figs 2-3; 6C-6I); and a transistor having first and second source/drain connections 38,28 and a gate connection, the gate connection connected to the further polysilicon 34 and the word line 4 (Figs 2-3; paragraphs 47-48,49-50), one of the first and second source/drain connections connected to the doped region and the bit line of the other one of the first and second source/drain electrically connected to the polysilicon that fills the bottom region of the deep trench that comprises the second plate of a memory cell capacitor (Figs 2-3). Re claim 47, the structure further comprising: a transistor having first and second source/drain connections 38,28 and a gate connection 34, the gate connection connected to the further polysilicon and the word line 4, one of the first and second source/drain connections connected to the doped region 38

and the bit line of the other one of the first and second source/drain electrically connected to the polysilicon that fills the bottom region of the deep trench that comprises the second plate of a memory cell capacitor (Figs 2-3; paragraphs 46-50). Re claim 48, wherein the doped region 38 is the first source/drain, the buried strap 28 is the second source/drain, and further polysilicon 34 is the gate of a vertical transistor (Figs 2-3; paragraphs 46-50). Re claims 49-51, wherein at least two deep trench structures 20 are separated by a distance 3F, where F is a minimum feature size (Fig 2).

Arnold already teaches forming at least two deep trench structures having the first trench collar portion 30 and the second trench collar portions 30 extending along the middle region of the sidewalls (Figs 2-4B). Arnold, however, lacks forming only the second trench collar portion extending along the second sidewall of both the middle and upper regions (claim 7).

However, Mandelman teaches a memory cell structure comprising at least two deep trench structures 24,26 and along one of the rows (Figs 5, col 5, lines 20-52; Figs 1), wherein the deep trench having first and second sidewalls extending along a bottom region, a middle region, and an upper region, wherein a first trench-collar portion 30 extending along the first sidewalls of the middle region and a second trench-collar portion 28 extending along the second sidewalls of both the middle and upper regions.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell structure of Arnold by forming only a second trench-collar portion extending along the second sidewalls of both the middle and upper regions, as taught by Mandelman. This is because of the desirability to form a single buried strap region on one side of the deep trench structure, thereby decreasing size of the memory structure and thus increasing array density.

Response to Amendment

3. Applicant's remarks filed March 29, 2006 with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-18

Michael Trinh
Primary Examiner